(12) **United States Patent**   (10) **Patent No.:**   **US 9,411,390 B2**

Smith et al.   (45) **Date of Patent:**   **Aug. 9, 2016**

(54) **INTEGRATED CIRCUIT DEVICE HAVING POWER DOMAINS AND PARTITIONS BASED ON USE CASE POWER OPTIMIZATION**

(75) Inventors: **Brian Smith**, Mountain View, CA (US); **Parthasarathy Sriram**, San Francisco, CA (US); **Stephane Le Provost**, San Jose, CA (US)

(73) Assignee: **NVIDIA CORPORATION**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 797 days.

(21) Appl. No.: **12/029,404**

(22) Filed: **Feb. 11, 2008**

(65) **Prior Publication Data**

US 2009/0201082 A1   Aug. 13, 2009

(51) **Int. Cl.**
G06F 1/32   (2006.01)
(52) **U.S. Cl.**
CPC *G06F 1/3203* (2013.01); *G06F 1/3287* (2013.01); *Y02B 60/1282* (2013.01)
(58) **Field of Classification Search**
CPC .. G06F 1/3203; G06F 1/3287; Y02B 60/1282
USPC 713/321, 322, 324
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,868,832	A	9/1989	Marrington et al.
5,220,660	A	6/1993	Yoshizawa et al.
5,339,445	A	8/1994	Gasztonyi
5,471,189	A	11/1995	Dietz et al.
5,510,740	A	4/1996	Farrell et al.
5,517,441	A	5/1996	Dietz et al.
5,530,845	A	6/1996	Hiatt et al.
5,586,308	A	12/1996	Hawkins et al.
5,588,099	A	12/1996	Mogilevsky et al.
5,649,222	A	7/1997	Mogilevsky
5,659,687	A	8/1997	Kim et al.
5,687,382	A	11/1997	Kojima et al.
5,737,613	A	4/1998	Mensch, Jr.

(Continued)

FOREIGN PATENT DOCUMENTS

GB	2457170	8/2009
WO	20040102623	11/2004

OTHER PUBLICATIONS

Application as Filed; U.S. Appl. No. 12/101,028; Brian Smith; et al., filed Apr. 10, 2008.

(Continued)

Primary Examiner — Thuan Du

(57) **ABSTRACT**

A programmable SoC (system on a chip) having optimized power domains and power islands. The SoC is an integrated circuit device including a plurality of power domains, each of the power domains having a respective voltage rail to supply power to the power domain. A plurality of power islands are included within the integrated circuit device, wherein each power domain includes at least one power island. A plurality of functional blocks are included within the integrated circuit device, wherein each power island includes at least one functional block. Each functional block is configured to provide a specific device functionality. The integrated circuit device adjusts power consumption in relation to a requested device functionality by individually turning on or turning off power to a selected one or more power domains, and for each turned on power domain, individually power gating one or more power islands.

22 Claims, 6 Drawing Sheets